Role of Charge Traps in the Performance of Atomically Thin Transistors

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Transient currents in atomically thin $MoTe_2$ field-effect transistors (FETs) are measured during cycles of pulses through the gate electrode. The curves of the transient currents are analyzed in light of a newly proposed model for charge-trapping dynamics that renders a time-dependent change in the threshold voltage as the dominant effect on the channel hysteretic behavior over emission currents from the charge traps. The proposed model is expected to be instrumental in understanding the fundamental physics that governs the performance of atomically thin FETs and is applicable to the entire class of atomically thin-based devices. Hence, the model is vital to the intelligent design of fast and highly efficient optoelectronic devices.

The emerging family of atomically thin materials is fueling the development of conceptually new technologies[1] in highly efficient optoelectronics[2,3] and photonic applications,[4] to name a few. The large variety of bandgap values found in layered transition-metal dichalcogenides (TMDCs)[5,6] make these materials especially suited for transistor applications. TMDCs are compounds with the general formula MX_2, where M is a transition metal, e.g., Mo and W, and X is an element of the chalcogen group, S, Se, and Te. They appear in a layered structure where the metal forms a hexagonal plane and the chalcogenides are positioned over and under this plane in either a trigonal prismatic (2H), as shown in **Figure 1**a, or octahedral (1T) stacking configuration.[7] In the semiconducting 2H systems, the compounds show a transition from indirect bandgap in bulk materials to direct bandgap in single layers.[8]

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Single- and few-layered TMDCs have been implemented in a wide range of applications, ranging from thin film transistors,[9] digital electronics and optoelectronics,[2,10,11] flexible electronics,[12] and up to energy conversion and storage devices.[13] However, the defect states in TMDCs have an ambivalent nature and can have a major positive or negative impact on the performance of atomically thin devices. The presence of defects in photodetectors can be beneficial since it has been shown to immobilize charges at the channel which improves the gain in photodetectors[14] and produces nonvolatile memory mechanisms.[15] On the other hand, large hysteresis caused, for example, by charge traps[2] and significant Schottky barriers[16] at the metal–semiconductor interface are still a major design challenge for the realization of novel device architectures. They have been shown to cause degradation in the performance of transistors[17] and generate high levels of flicker noise.[18,19] To overcome these challenges, hysteresis is usually avoided by encapsulation[20,21] or operation under high vacuum.[22,23]

Most of the current research into surface states of TMDCs has focused on the chemical origins of charge trapping. A full understanding of their effect on the electrical properties is still lacking, hindering the optimization of functional components. While hysteresis has been shown to correlate with traps generated at the channel–dielectric interface and the channel–ambient interface,[24,25] little attention has been given to the mechanisms by which immobile charges affect the conduction characteristics of the devices, which is fundamentally different from those experienced in bulk devices.

Here, we present the first study of the role of immobile charges on the electrical transport properties of atomically thin $MoTe_2$. This TMDC is of particular interest since its direct bandgap of 1 eV[26,27] matches the wavelength of maximal solar emission intensity, thus making it a prime candidate for solar energy converters. $MoTe_2$ is intrinsically p-doped, but can exhibit ambipolar behavior,[26,28] mobility in the range of 10^{-30} cm^2 V^{-1} s^{-1},[26,29] and on–off ratios of up to 10^6.[29] A stringent quantitative analysis demonstrates that the role of trapped charges in the operation of $MoTe_2$-based electronic components is a change in the threshold voltage of the field-effect transistor (FET), effectively modulating the resistivity of the entire channel. By repeating the charge capture and emission cycles in different drain biases we are able to distinguish between two sources of transient behavior in $MoTe_2$ FETs. One transient is due to emission of charges from traps to the channel, and the other is due

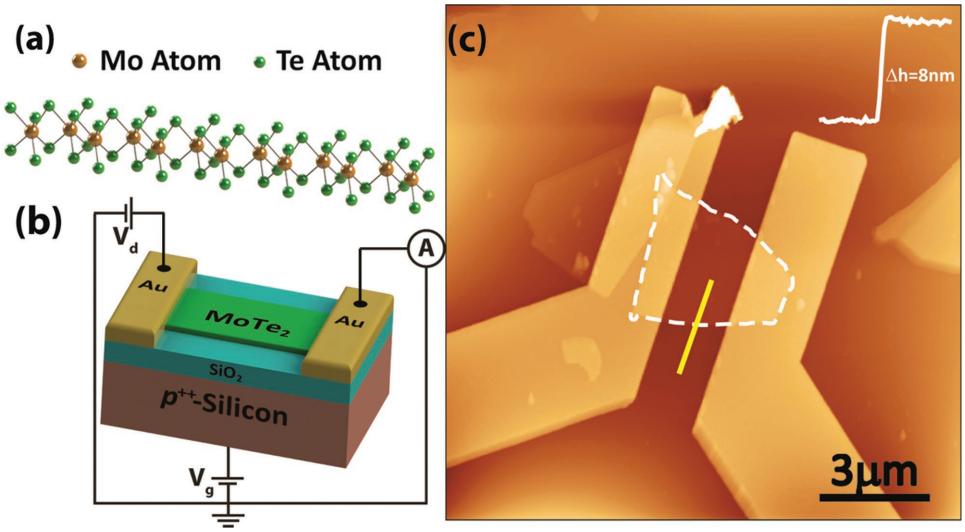

Figure 1. a) A 3D model of the 2H-$MoTe_2$ crystal structure, with a single layer of the trigonal prismatic stack. b) Schematics of the device architecture and measurement setup. c) Atomic force microscopy image of a typical device, showing the source and drain symmetric electrodes and the $MoTe_2$ flake (outlined in dashed white line). The inset shows a scan profile (taken along the yellow line) from the substrate to the flake.

to time-dependent capacitive gating of the channel that produces a transient in the effective threshold voltage. Finally, we present a complete analytical model to support our observations. Our findings are applicable to the entire class of atomically thin-based devices and provide a thorough understanding of charge traps and carrier dynamics which is needed to facilitate the intelligent design of fast and highly efficient optoelectronic devices.

Few-layered $MoTe_2$ flakes were obtained by mechanical exfoliation of 2H-$MoTe_2$ bulk crystal (HQ graphene) onto highly doped silicon substrates, covered with 290 nm of high-quality thermally grown SiO_2. The silicon substrate was used as a global back gate electrode, with the oxide layer acting as a gate dielectric. Standard electron beam lithography procedure was used to pattern electrodes and electrical leads. The contacts were then immediately metalized with 5 nm of Ti adhesion layer, and 50 nm of Au, using an electron beam evaporation system, working at very low pressure (≈10^{-8} mbar) and at long working distance, to achieve high uniformity in the deposition. The devices were then annealed in dry Ar/H_2 environment at ambient pressure for 2 h at 200 °C. Figure 1b shows a schematic representation, not to scale, of the device and the circuit details. Atomic force microscopy measurements (Figure 1c) and optical contrast (not shown here) of the flakes confirm that the surface of $MoTe_2$ is not visibly contaminated and that the studied flakes consist of four layers.

Low-noise electrical measurements were performed in a home-built Faraday cage in the dark and in ambient conditions on more than five different devices, all showing a similar behavior. The drain electrode was biased using a low-noise voltage source and the source electrode was kept grounded throughout the experiment. The current flowing through the source electrode was measured using a current preamplifier. An independent voltage source-meter was used to apply a bias to the gate electrode while measuring the leakage current. The response time of the system was found to be limited only by the minimal rise time of the preamplifier, which is <5 μs (see the Supporting Information).

The electronic behavior of multiple devices was characterized by measuring their drain current versus voltage response (I_{ds}–V_{ds}) and drain current versus gate voltage transfer (I_{ds}–V_{gs}) characteristics. **Figure 2**a shows the response curve of a typical $MoTe_2$ transistor. The curve exhibits a slight asymmetry with higher resistivity for negative applied drain bias, indicating that the metal–semiconductor contacts form a small Schottky barrier for holes. The origin of this asymmetry about $V_{ds} = 0$ V is in the different electrostatic potential seen by the source and drain electrodes. In the experiment the potential barrier at the $MoTe_2$/source electrode interface is kept constant, as it is pinned by the gate. On the other hand, the biased drain barrier decreases (increases) in height with positive (negative) drain bias.[30] Despite the low Schottky barrier, both the linear and the log-scale of the response curve (inset in Figure 2a) show that the device is not rectifying and is, in fact, largely Ohmic in higher V_{ds} values (see the Supporting Information).

The device transfer characteristics are shown in Figure 2b, taken at $V_{ds} = 1$ V. The curve matches the expected behavior of an enhancement-mode *p*-channel transistor, showing an increase in drain current as the gate bias grows more negative beyond the threshold voltage (V_{th}). From the transfer curve, we can estimate the device mobility, μ_p, and subthreshold swing, SS. Using $\mu_p = L(dI_{ds}/dV_{gs})/(WC_{ox}V_{ds})$ in the linear regime of the curve, where $L = 1$ μm and $W = 3$ μm are the device length and width, respectively, and $C_{ox} = \varepsilon_0\varepsilon_r/d = 115$ μF m^{-2} is the gate dielectric capacitance, with ε_0 the vacuum permittivity, and ε_r the oxide relative permittivity, we find that the mobility is between 0.12 on the forward sweep and 0.14 cm^2 V^{-1} s^{-1} on the back sweep. From the subthreshold part of the curve, we estimate a subthreshold swing value of 4 V dec^{-1} using $SS = (d\log_{10}I_d/dV_g)^{-1}$. The low value of the mobility and the high value of the swing are indicative of the presence of midgap trap states.[14] In line with these findings, the gate sweep measurements also show a hysteretic behavior resulting in a shift in V_{th} between the forward and backward sweeps, which changes

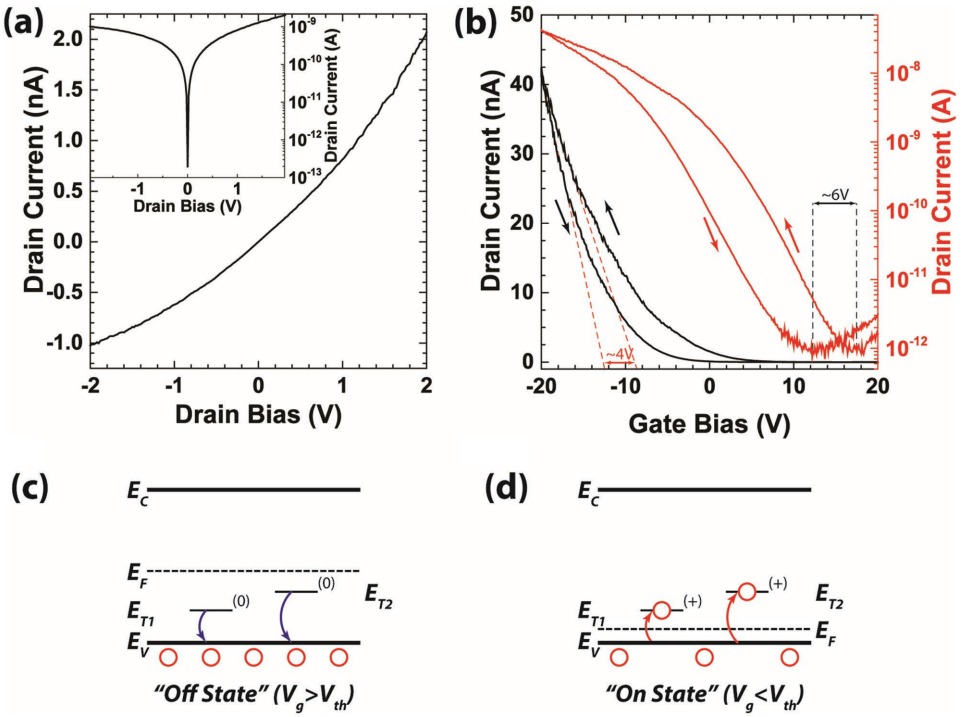

Figure 2. Panel (a) shows the response (I_{ds}–V_{ds}) curve of a typical field-effect transistor, taken with zero gate bias ($V_{gs} = 0$). The inset shows the same curve in a semi-logarithmic scale. Panel (b) shows the transfer (I_{ds}–V_{gs}) curve of the same device taken with 1 V source drain bias (V_{ds}) shown in a linear (solid black) and semi-logarithmic (solid red) scale. The dashed red lines are a linear extrapolation of the linear part of the curve, showing a change of 4 V in threshold voltage. The dashed black lines indicate the change in the position of the charge neutrality point. The arrows indicate the back gate sweep direction. Panels (c) and (d) show schematic energy band diagrams for the emission (c) and capture process (d) when the channel is in the "off state" and "on state", respectively. E_C, E_V, E_F, E_{T1}, and E_{T2} are the conduction-band minimum, the valance-band maximum, the Fermi energy, the shallow midgap state, and deep midgap state energy, respectively.

the threshold voltage by about $\Delta V_{th} = -4$ V and the charge neutrality point by about –6 V, see Figure 2b.

To understand the physical origin of the observed changes in threshold voltage, we use the well-known equation that describes V_{th} in field-effect transistors:

$$V_{th} = \phi_{MS} - \frac{Q_i}{C_{ox}} - \frac{Q_T}{C_{ox}} - \Delta E_F \quad (1)$$

where ϕ_{MS} is the difference between the metal and semiconductor work functions when all the terminals are grounded, C_{ox} is the gate dielectric capacitance, Q_i is the static charge density within the dielectric, Q_T is the trapped charge density at the interface between the dielectric and the conductive channel, and ΔE_F is the shift in the Fermi energy, required to turn the transistor on. From Equation (1), it is clear that the only parameter that can change during the back gate sweep is the population of midgap traps, Q_T, indicating that positive charges (holes) are immobilized during the sweep. The process of charge trapping is illustrated in the energy band diagrams of Figure 2c,d using two "donor-type" midgap states. In the "off state", where the Fermi level is above the trap levels (E_{T1} and E_{T2}) the traps are occupied by an electron and are neutral. In the "on state", the traps are void of electrons (occupied by a hole) and are positively charged.

A priori, the observed hysteresis can be due to charge trapping in the metal–semiconductor interface, i.e., localized at the contacts region, or at the entire surface area of the channel, i.e., at the semiconductor–dielectric and semiconductor–ambient interface. However, the changes in the transfer curve strongly suggest that most of the charge trapping occurs throughout the entire area of the conductive channel, rather than at the metal–semiconductor interface. The noticeable shift in the charge neutrality point with respect to the gate bias (minimal conductivity in the log-scale, red curve) in Figure 2b, is indicative of a change in effective doping of the channel due to the space charge region generated by the immobilized charges. In contrast, a change in the degree of Fermi-level pinning at the contacts would have manifested primarily in changes in the linear slope of the logarithmic curve (the subthreshold slope) and by changes in the width of the neutrality point. Assuming that the trapped charges are distributed in the channel, an assumption that is further validated by the analysis of the threshold transients, we can estimate that the difference in trapped charge density between the forward and back sweep is about 4.3×10^{11} cm^{-2}, using $\Delta Q_T = VC_{ox}$.

To gain insight on the dynamics of the charge traps, their effect on the transfer currents and their role in producing hysteretic cycles, we have monitored the transport characteristics while pulsing the gate electrode from "open" (more negative) to a "close" (more positive) value. The drain current was recorded over long periods of time (60–90 min) while the gate was repeatedly pulsed between $V_{gs} = -10$ V to open the channel and

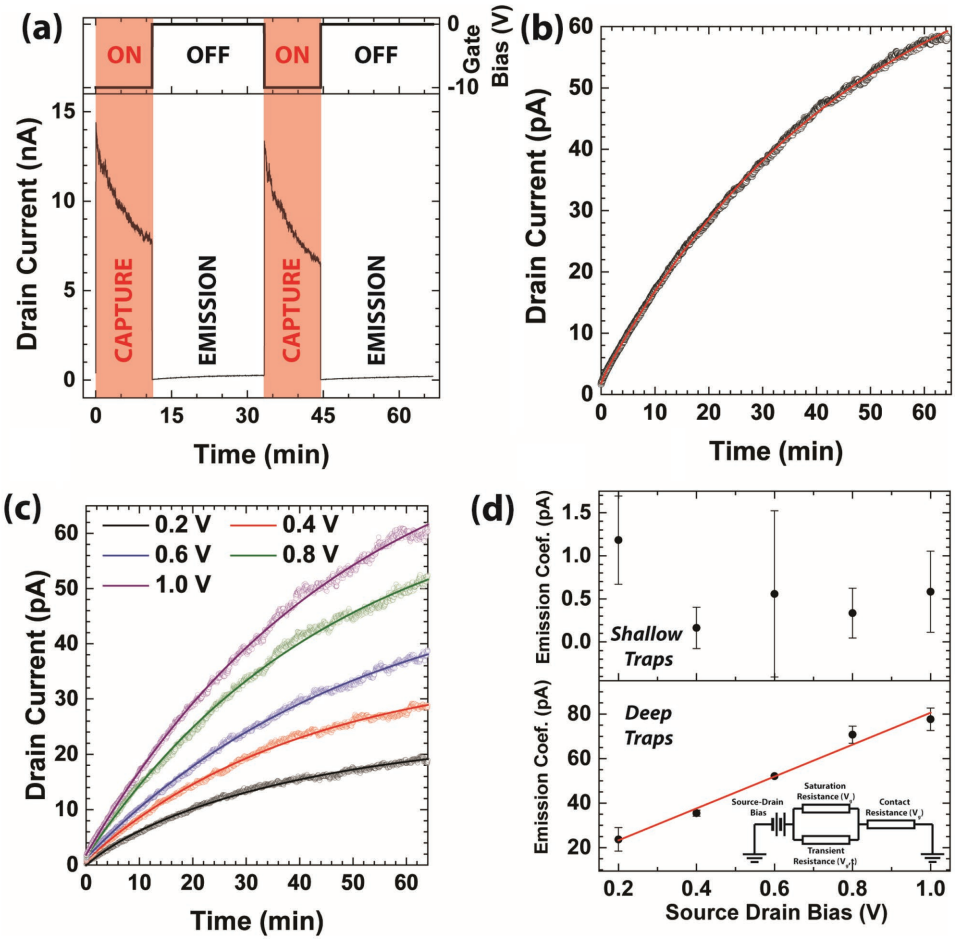

Figure 3. a) Gate pulse cycles. The "On" and "Off" segments are highlighted. On the top, the applied gate voltage during each segment. On the bottom panel: The drain current during the capture (on red background) and emission (on white background) segments. b) An emission segment, recorded at V_{gs} = 0 V and V_{ds} = 1 V, averaged over four cycles. The black circles are the measured data and the red curve is the fit to a double-exponential rise equation. c) Emission segments, recorded at V_{gs} = 0 V and varying V_{ds} values, from 0.2 to 1.0 V in 0.2 V intervals. The circles are the measured data and the solid curves are the double-exponential fits. d) The pre-exponential coefficients for the short emission coefficient, A_1 (top panel) and long emission coefficient, A_2. The red line represents the best linear fit. Inset: An equivalent circuit diagram of the transient threshold model proposed here.

V_{gs} = 0 V to close it (top panel in **Figure 3**a). As the pulse on gate drives the channel from a close to an open state, a sudden rise of the current in the channel is measured followed by a fast decay. When the gate is pulsed back to the closed state, the current drops down and then slowly begins to recover. The decay in current in the open state is due to the capturing of holes in midgap traps that shifts the threshold voltage to a more negative value (red arrows in Figure 2d), effectively closing the channel. On the other hand, the recovery in the off state is due to the holes that are emitted from the traps (blue arrow in Figure 2c) shifting V_{th} to a less negative value. While the capture process is spontaneous and fast, the emission mechanism is thermally activated and, therefore, significantly slower than the capture rates.

The vast majority of models used to quantify the time-dependent behavior of charge emission from midgap traps are based on Schottky or asymmetric diode structures.[31,32] These models accurately describe the currents, and the resulting transient changes in capacitance, that are associated solely with the emission of charges from traps back into the circuit. However, transient changes in threshold voltage should affect the measured current in a completely different way, which has not yet been studied though it plays a pivotal role for the development of fast optoelectronic applications.

To elucidate the fundamental difference in transient behaviors, we must first describe the main aspects of the conventional semiconductor model for current transients. When the emission of charges from depletion regions takes place, the current has a constant (saturation) component, which is a function of the applied bias, and a transient component which is the emission current:

$$I(t) = I_0 + \frac{qN_T A}{\tau} e^{-t/\tau} \quad (2)$$

I_0 is the saturation current, q is the elementary charge, and A is the surface area of the device contact. Within this model, the time dependence of the transient current is a function of the density of trapped charges (N_T) and the decay coefficient τ which is a function of the energetic position of the trap with

respect to the valance band (see the Supporting Information). However, in atomically thin $MoTe_2$ FET, the high sensitivity of the conducting channel to its surrounding media means that the charge carrier dynamics can lead to significant shifts in threshold voltage and charge neutrality point, effectively changing the resistance of the entire channel. Hence, an inclusive model in which the resistivity changes with time is needed. To this end, we use the well-known expression that describes the linear regime of the transfer curve, where the current is determined by:[33]

$$I_d(t) = \frac{W\mu_p C_{ox}}{L}\left(V_{th}(t) - V_g\right)V_d \tag{3}$$

where W and L are the channel width and length, respectively, and μ_p is the hole mobility. Since in atomically thin FETs, the only time-dependent component of the threshold voltage (Equation (1)) is the density of trapped charges we can write $dV_{th}(t)/dt = -(q/C_{ox})(dp_T(t)/dt)$ where $p_T = Q_T/q$ is the density of occupied traps. To obtain a full description of the threshold voltage transient, $V_{th}(t)$, we assume that the density of free carriers, p, directly correlates to the equilibrium density p_0, by $p = p_0 - p_T$, i.e., that there is no net injection of charges through the contacts. We further use the well-known result of the Shockley–Reed–Hall derivation to write the time-dependent density of occupied traps as $p_T = N_T e^{-t/\tau}$. The transient of the threshold voltage then becomes:

$$V_{th}(t) = V_{th,sat} - \frac{qN_T e^{-t/\tau}}{C_{ox}} \tag{4}$$

where all the time-independent quantities have been grouped in $V_{th,sat}$ for convenience. With the expression for $V_{th}(t)$ from Equation (4), the expression for the transient current is readily obtained:

$$I_d(t) = I_{d,sat} - \frac{qW\mu_p N_T V_d}{L} e^{-t/\tau} \tag{5}$$

The expression in Equation (5) has one striking difference from the conventional expression for current transient (Equation (2)), it is linear with drain bias. Qualitatively, this is a simple manifestation of Ohm's law: as the resistance of the conductive channel changes with time, the current responds linearly, proportional to the applied bias.

In the emission segments of the gate-pulse experiment, we find that a significant increase in currents occur on a very short time scales, while a further, slower increase is easily discernible in longer time scales. This behavior cannot be satisfied by a single exponential fit but is in excellent agreement with a double exponential rise equation in the form $I(t) = I_0 + A_1 e^{-t/\tau_1} + A_2 e^{-t/\tau_2}$ (red line in Figure 3a) suggesting that there are two types of traps,[25] a shallow trap and a deeper one, corresponding to emission coefficients $\tau_1 \approx 250$ s and $\tau_2 \approx 2900$ s. Figure 3b shows the recovery currents, measured by pulsing the gate between −10 and 0 V at drain bias values ranging from 0.2 to 1 V. The curves are then fitted with a double exponential rise curve, without any assumption on the form of the pre-exponential factors, A_1 and A_2, while maintaining the emission constants within reasonable boundaries.

To distinguish between the different contributions to the transient current, the pre-exponential factors of the shallow and deep traps are plotted in Figure 3d on the top and bottom panel, respectively. Within the measurement error, it is clear that the pre-exponential factor of the transient current that is due to emission from the shallow traps is constant, and independent of the drain bias. This suggests that the measured signal is, indeed, the emission current from the traps. For the deep traps, the pre-exponential factors are found to have a linear dependence on V_{ds}. This is expected for deep traps that are uniformly distributed about the conductive channel and are not simply concentrated at the metal–semiconductor interface, and is consistent with the analysis of the hysteresis of the gate bias measurements. Comparing the two panels in Figure 3d reveals two striking features in the transient mechanism. First, the two orders of magnitude difference in the pre-exponential coefficients shows that the threshold transient is the significant factor, governing the transistor response over time. Second, the change in the trap population ($\Delta N_T = L(dA_2/dV_d)/(qW\mu_p) \approx 10^9$ cm^{-2}) is a small fraction of the overall estimated density of 10^{12} states per cm^2,[34] corresponding to the small dynamic window of operation used here. This emphasizes the significant role that the threshold voltage transients play in the behavior of atomically thin $MoTe_2$ transistors.

The presented model of the threshold voltage transients is general, since it does not take into account features which are specific to $MoTe_2$. For example, similar studies conducted on WS_2 grown by chemical vapor deposition also show a biexponential decay of the transient current which is fully captured by our model (see the Supporting Information). Most importantly, this model is independent of the spatial location of trapped charge states (e.g., semiconductor–substrate or semiconductor–ambient interface) and it is universally valid for semiconductor channels thickness that are significantly smaller than the Debye screening length, a condition easily met in emerging atomically thin materials. Our proposed model of threshold voltage transients can be further expanded and included in well-established methodology of charge trap spectroscopy, whether probed by temperature scans[35] or by optical means.[36] However, the added simplicity of our methodology means that it can be applied to a variety of materials and substrates, including those that are photoactive, or temperature sensitive.

Finally, we calculate the overall resistance of the device and find that the transient resistance operates in parallel to the saturation resistance:

$$\left(\frac{dI_d(t)}{dV_d}\right) = \left(\frac{dI_{d,sat}(t)}{dV_d}\right) - \frac{qW\mu_p N_T}{L} e^{-t/\tau} \tag{6}$$

or $R^{-1} = R_{sat}^{-1} + R_{trans}^{-1}$ which is a strong indication to the fact that both factors indeed stem from the channel itself. We note that the addition of series resistance to the circuit, such as contact resistance, does not affect the time-dependent characteristics of the model, as is discussed in detail in the Supporting Information.

In conclusion, we have demonstrated a new approach to the analysis of charge trapping and transient response of TMDC-based FETs, which paves the way to a better understanding of

the role of midgap states in the operation novel devices. Using a simple two terminal model system, we were able to distinguish between currents associated with the emission of trapped charges into the circuit and currents that evolve in time due to the changes in effective threshold voltage across the channel. The mechanism of threshold voltage transients which we study and model is not limited to $MoTe_2$ but it is valid to any device based on atomically thin materials. Indeed, as long as the channel depth is much smaller than the Debye screening length, the threshold voltage will be strongly modulated by the formation of space charge regions at both the semiconductor–dielectric and semiconductor–ambient interfaces. Our model, which describes the basic physics that govern the hysteretic characteristics of atomically thin FETs, is instrumental for the design of defect-based devices, such as photodetectors and memory devices, as well as provides a new methodology to study the nature of these defects.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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